PCB Layout and Design Guide for CH7036 RGB/HDMI/LVDS Encoder

1.0 Introduction

The CH7036 is specifically designed for consumer electronics device and PC markets in which multiple high definition content display formats are required. With its advanced video encoder, flexible scaling engine and easy-to-configure audio interface, the CH7036 satisfies manufactures' products display requirements and reduce their costs of development and time-to-market.

This application note focuses only on the basic PCB layout and design guidelines for CH7036 RGB/HDMI/LVDS Encoder. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 88-pin QFN package of the CH7036. Please refer to the CH7036datasheet for the details of the pin assignments.

2.0 Component Placement and Design Considerations

Components associated with the CH7036 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These 0.1μF capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7036 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7036 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7036 ground pins should be connected to its respective decoupling capacitor ground lead directly, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

There are nine power supply pins, VDDH, VDDR, VDDT, DVDD, AVDD, AVDD_PLL, AVDD_DAC, VDDMQ, VDDMS. Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7036

Pin Assignment	# of Pins	Type	Symbol	Description
11,12	2	Power	VDDH	HDMI supply voltage (3.3V)
23	1	Power	VDDR	LVDS Input supply voltage (3.3V)
40	1	Power	VDDT	LVDS Output supply voltage (3.3V)
19,57	2	Power	DVDD	Digital supply voltage (1.8V)
46,79	2	Power	AVDD	Analog supply voltage (2.5V~3.3V)
1,20	2	Power	AVDD_PLL	PLL supply voltage (1.8V)
69,73	2	Power	AVDD_DAC	DAC power supply (2.5~3.3V)

54,62	2	Power	VDDMQ	SDRAM output buffer supply voltage (3.3V)
4,61	2	Power	VDDMS	SDRAM device supply voltage (3.3V)
6,17	2	Ground	VSSH	HDMI supply ground
22	1	Ground	VSSR	LVDS Input supply ground
45	1	Ground	VSST	LVDS Output supply ground
18,56	2	Ground	DGND	Digital supply ground
50,82	4	Ground	AGND	Analog supply ground
2,21	2	Ground	AGND_PLL	PLL supply ground
71,75	2	Ground	AGND_DAC	DAC supply ground
55,63	2	Ground	GNDMQ	SDRAM output buffer supply ground
5,60	2	Ground	GNDMS	SDRAM device supply ground
Thermal Exposed Pad		Ground		Connect to ground plane through thermal via

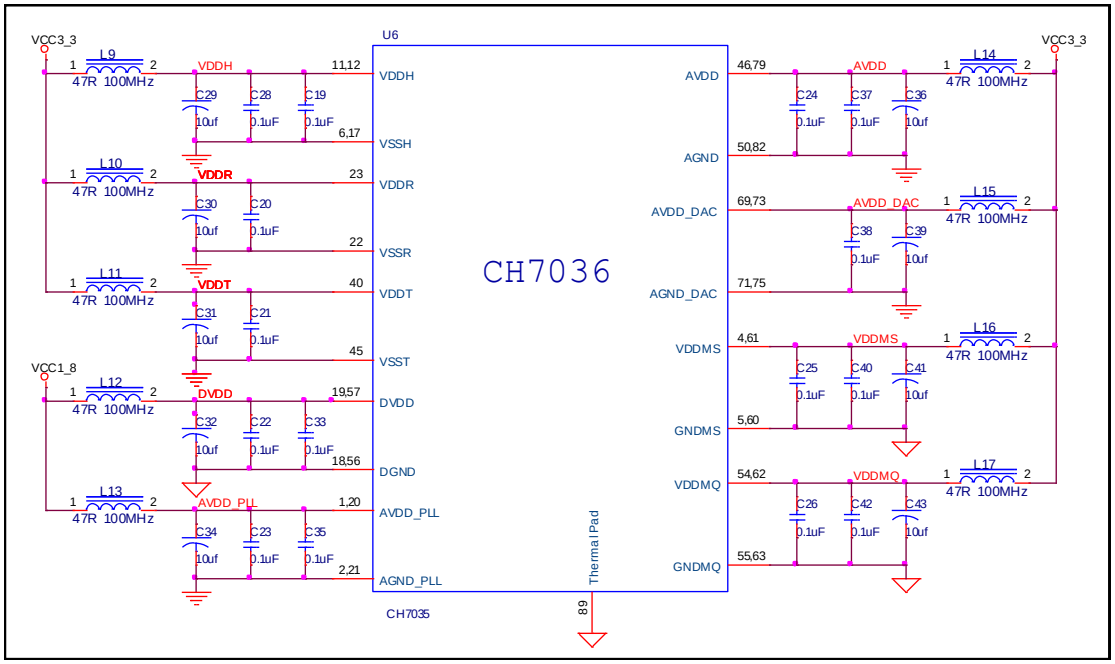


Figure 1: Power Supply Decoupling and Distribution

Note: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05 Ω at DC; 23 Ω at 25MHz & 47 Ω at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.

2.2 Power On and Reset

RSTB pin is the chip reset pin of CH7036. CH7036 will be reset when this pin is low. A power reset switch can be placed on the RSTB pin on the PCB as hardware reset for CH7036 as shown in **Figure 5**. When the pin is high, the reset function can also be controlled through the serial port.

There are two reset methods. One is RC reset. The power supply should be valid and stable for at least 9ms before RSTB becomes invalid as shown in **Figure 2**. A 1 MΩ and 0.1uF RC reset circuit is recommended.

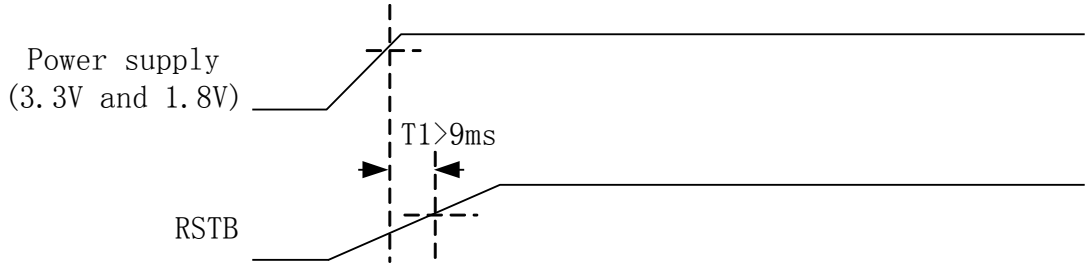


Figure 2: Power on and reset timing of RC

Another method is using an external reset signal. In this case, the power supply should be valid and stable for at least 9ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. The timing is shown in **Figure 3.**

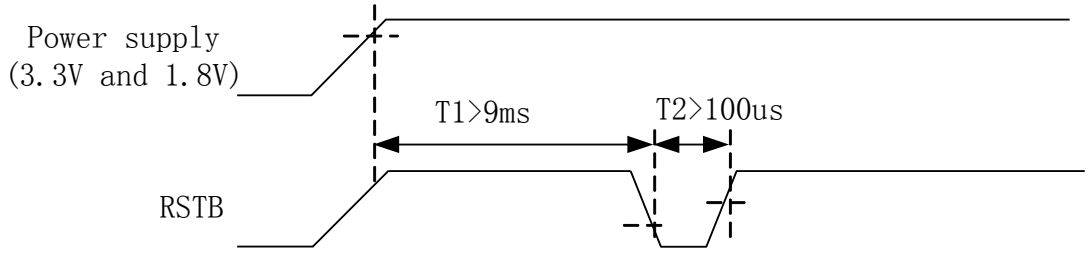


Figure 3: Power on and reset timing of external reset

Note: 1. The power supply will be valid when it rises to 90% of standard level.
2. The rising threshold of RSTB is 2.4V.
3. The falling threshold of RSTB is 0.4V.

2.3 General Control Pins

• ISET and RESERVED

ISET pin sets the DAC current. A 1.2 KΩ, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces as shown in **Figure 4.**

The RESERVED pins (Pin3 and Pin66) should be pulled low through 10 KΩ resistors.

• GPI1, GPI2 and PDB

GPI1 and GPI2 can be used as input pins controlled by MCU.

PDB controls to power down the whole chip when it is low. After PDB pin is pulled high again, the CH7036 will be reset.

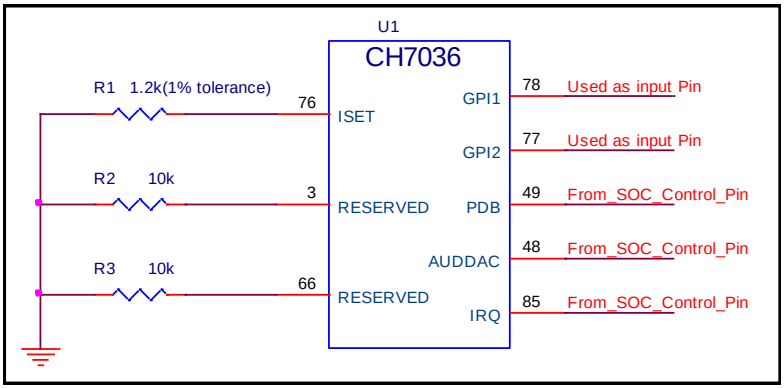


Figure 4: General Control Pins (A)

• AUDDAC and IRQ

AUDDAC is Audio control output pin. This pin should be connected to SOC directly.

IRQ is Interrupt output pin. This pin should be connected to SOC directly. This Pins' default output is 3.3V CMOS level, and can also work as open drain structure for other voltages.

• XI and XO

If only using RGB output mode, CH7036 has capability to accept external clocks with frequencies from 2.3 MHz to 64 MHz. However, if using HDMI output mode, the crystal must be 27MHz.

The crystal load capacitance, C_L, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors **Figure 5** gives a reference design for crystal circuit design.

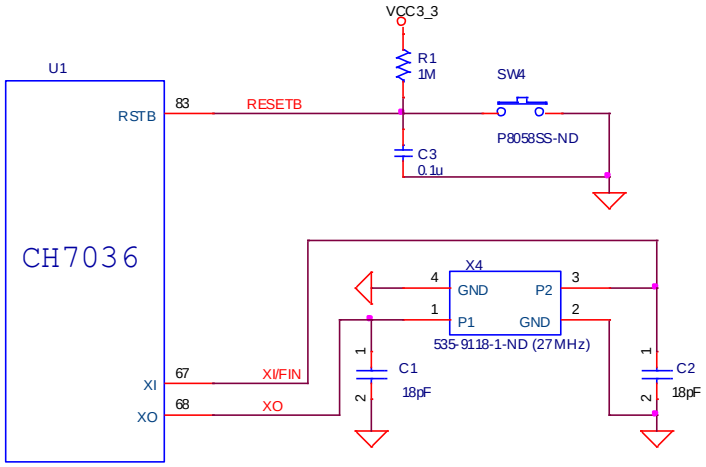


Figure 5: General Control Pins (B)

• Reference Crystal Oscillator

CH7036 includes an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7036. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±50 ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±50 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7036 (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$\mathbf{C}_{ext} = (2 \times C_L) - C_{int} - 2C_S$

Where

C_{ext} = external load capacitance required on XI and XO pins.
C_L = crystal load capacitance specified by crystal manufacturer.
C_{int} = capacitance internal to CH7036 (approximately 10-15 pF on each of XI and XO pins).
C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

such that $C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int} = 2C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int} /2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

2.4 Serial Port Control for CH7036

• SPC and SPD

SPD and SPC function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC pins are pulled up to AVDD with 5.6 KΩ resistors as shown in **Figure 6**. If the driver can support, SMBUS or LVDS DDC can be used to access CH7036 by the serial interface.

• DDC_SC and DDC_SD

DDC_SC and DDC_SD are used to interface with the DDC of HDMI receiver. This DDC pair needs to be pulled up to 5V through R3 and R4 as shown in **Figure 6**. R3 and R4's value should be from 1.5 KΩ to 2 KΩ according to the HDMI Specification. An EEPROM CH9903 can be added in DDC bus. The CH9903 is used to save the HDCP key in it, and its device address should not be 0x54.

• PROM_SC and PROM_SD

This Serial Port is used to load the firmware from external EEPROM CH9904. This serial pair needs to be pulled up to 3.3V through 10 KΩ resistors as shown in **Figure 6**. The CH9904 device address should be 0xAE.

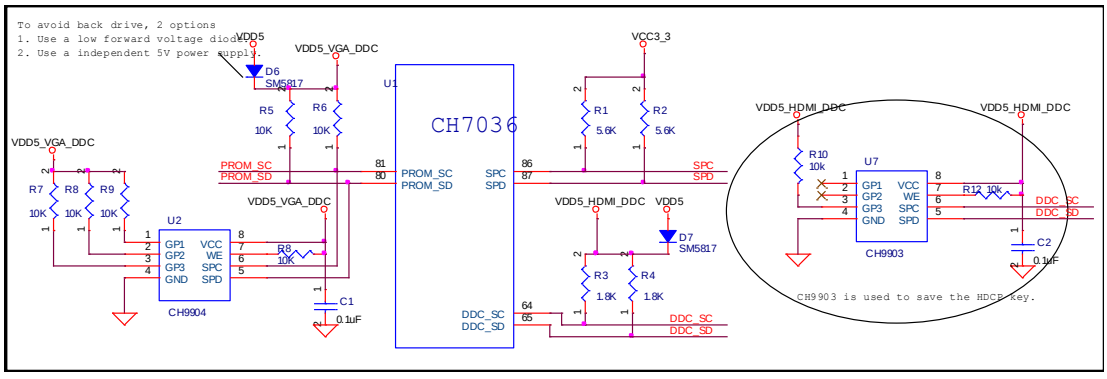


Figure 6: Serial Port Interface of CH7036

This Serial Port also can be used as the VGA DDC bus. They should be pulled up to 5V through 10 k Ω resistors as shown in **Figure 14.**

Note: Because some TV or monitor have internal 5V pull-up resistors on DDC trace, the 5V pull-up voltage will remain on DDC trace when TV or monitor is in standby mode. In order to avoid back drive, the power for DDC circuit of CH7036 should be independent 5V power supply. Using a diode with low forward voltage is another option. It is better that the forward voltage of the diode does not exceed 0.3V to avoid the voltage on pull-up resistors drops too low.

2.5 SPDIF Interface

IIS_D/SPDIF (pin 53) is a multi-function input pin. It can be configured to SPDIF audio input pin or IIS data input pin.
The SPDIF signal has two voltage levels, so there are two input ways for CH7036. If SPDIF signal from audio codec is COMS or TTL level (3.3V~5V), it can be connected to the CH7036 directly. If SPDIF signal is COAX level (0.5V~1V), a voltage level shifting is required as shown in **Figure 7**.

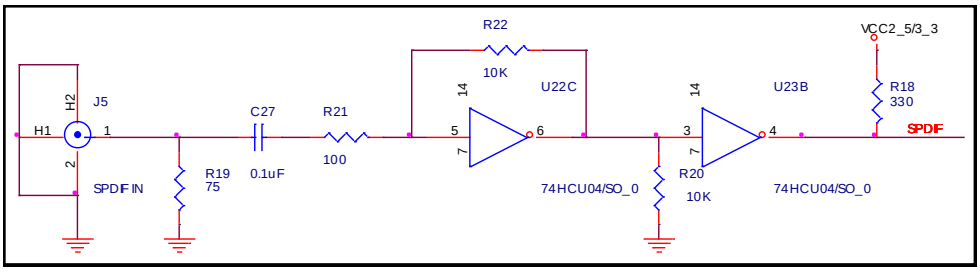


Figure 7: SPDIF pin of CH7036

Note1: It is recommended that 74HCU04 should be used.
Note2: For 74HCU04/SO, pin7=GND, pin14=VCC=2.5V or 3.3V.

2.6 I2S Interface

I2S audio input can be configured through programming CH7036 registers. An I2S bus design consists of three serial bus lines: a line with data channel [SD], a word select line [WS], and a clock line [SCK]. Data is transmitted two's complement, MSB first.

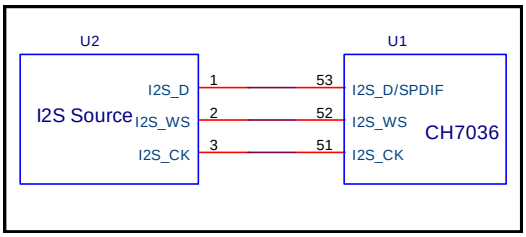


Figure 8: CH7036 I2S Input Pins

2.7 LVDS Input Pins

CH7036 can accept 18bit or 24bit SPWG format data from LVDS transmitter. As shown in **Figure 9**, Video data comes from a LVDS transmitter. Since those signals are differential, they must be routed in differential pairs.

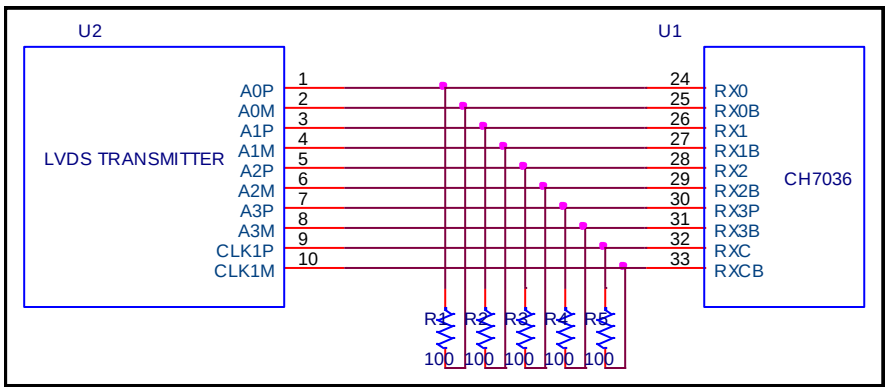


Figure 9: CH7036 Data Input Pins

The differential impedance of LVDS pairs should be 100Ω. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

CH7036 LVDS input channel differential pairs have Optional Internal termination resistors of 100Ω inside. It has the advantage of terminating as close as possible to the receiver (minimizing stubs) and also saving board space and reducing component count.

It is better to add a termination resistor (100Ω) between the differential pair for backup. The small surface mount termination resistors should be placed as close to the CH7036 input pins as possible.

CH7036 also support LVDS bypass mode as shown in **Figure 10**. When only output LVDS signal to Panel, CH7036 can be set to full power down mode to save the current. When using the CH7036 to output HDMI or VGA signal, the input LVDS pixel clock is up to 75HMz. The LVDS stub trace connected to CH7036 should less than 2 inches.

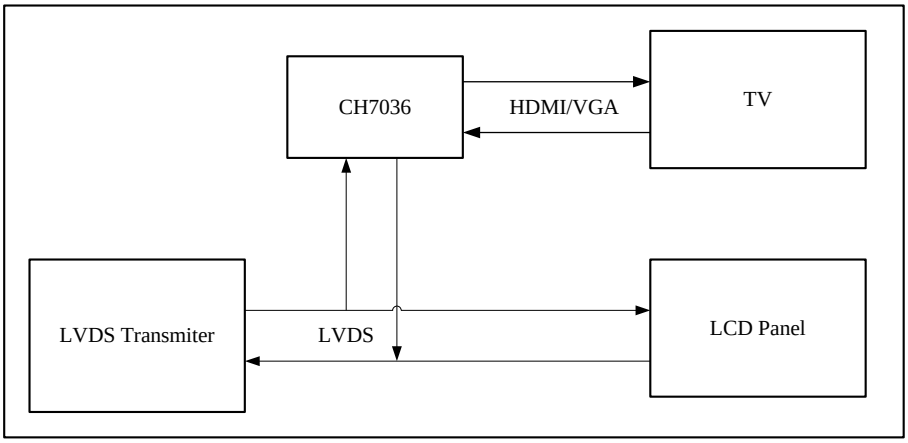


Figure 10: CH7036 LVDS bypass mode

2.8 HDMI Outputs

The TLC, TLCB, TDC [2:0], TDCB [2:0] signals are high frequency differential signals that need to be routed with special precautions. Since those signals are differential, they must be routed in differential pairs.

2.8.1 Differential Pair Impedance

To match the external cable impedance and maintain the maximal energy efficiency it is important to meet the impedance target of 100 Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc. The HDMI differential pairs should be routed on the top layer directly to the HDMI connector pads if possible.

2.8.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. Trace routing lengths from CH7036 to the HDMI/DVI connector are limited to a maximum of 2 inches. The CH7036 should be as close to the HDMI/DVI connector as possible.

2.8.3 Length Matching for Differential Pairs

The HDMI/DVI specifies the intra-pair skew and the inter-pair skew as in **Table 2**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement

signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

Table 2: Maximum Skews for the HDMI/DVI Transmitter

Skew Type	Maximum at Transmitter
Intra-Pair Skew	0.15 T_{bit}
Inter-Pair Skew	0.20 T_{Pixel}

Where T_{bit} is defined as the reciprocal of Data Transfer Rate and T_{Pixel} is defined as the reciprocal of Clock Rate.

Therefore, T_{Pixel} is 10 times T_{bit}. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment by segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 100 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

2.8.4 ESD Protection for HDMI/DVI Interface

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI Outputs (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel's recommended diode protection circuitry, using SEMTECH Rclamp0524P diode array devices, will protect the CH7036 device from HDMI panel discharges of greater than 8kV (contact) and 16kV (air). The RClampTM0524P have a typical capacitance of only 0.30pF between I/O pins. This low capacitance won't bring too much bad effect on HDMI eye diagram test.

Figure 11 shows the connection of HDMI connectors, including the recommended design of SEMTECH Rclamp0524P diode array devices. HDMI connector is used to connect the CH7036 HDMI outputs to the display panels.

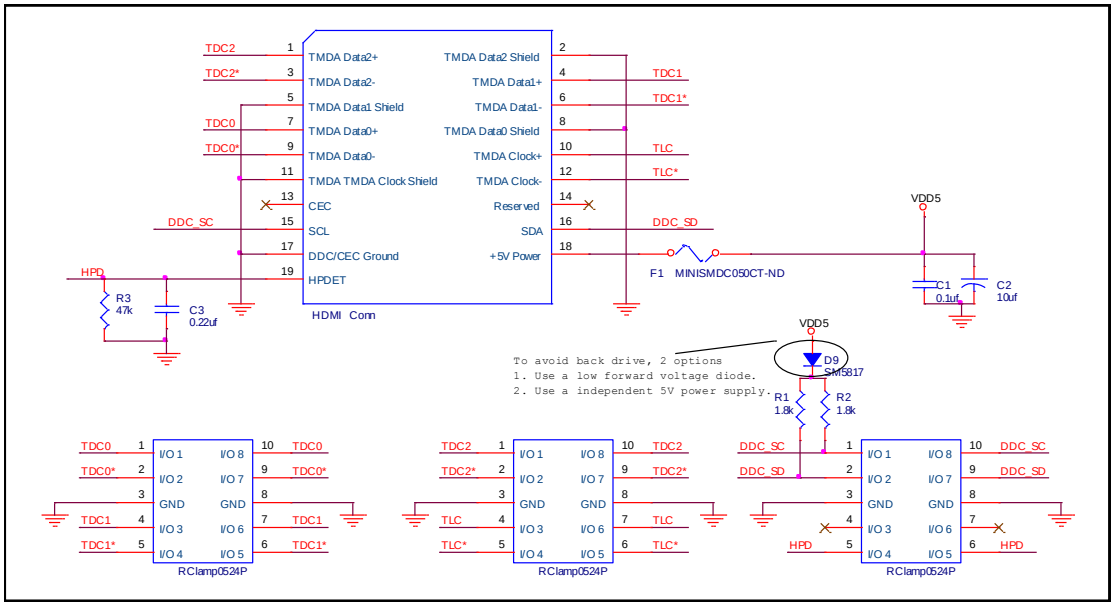


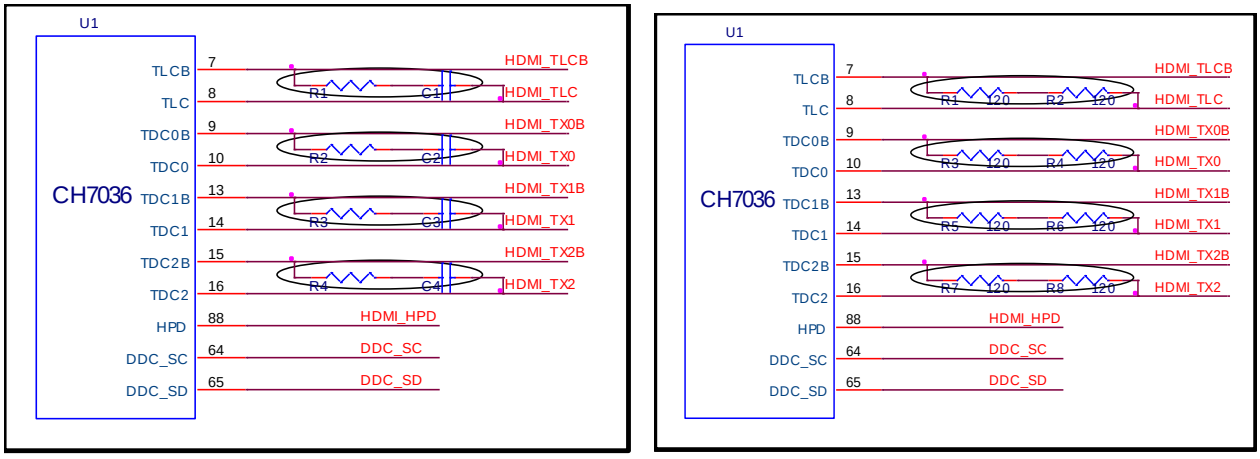
Figure 11: The connection of the HDMI outputs with ESD protection

2.8.5 Description for each HDMI Interface Pins

• HDMI Link Data Channel (TDC [2:0] and TDCB [2:0])

These pins provide HDMI differential outputs for data channel 0 (blue), data channel 1 (green) and data channel 2 (red). It is recommended that an impedance compensation circuit be added for each differential pair, including HDMI Clock outputs (Refer to **Figure 12**).

Figure 12(a) shows the RC bridge between the Differential pairs. These RC bridges can be optional soldered to prevent the EMI issue. It also can be used as impedance compensation to improve the HDMI eye diagram quality. A recommended bridge for all the data/clock differential pairs is with 240Ω resistance value as shown in **Figure 12(b)**. Please note that the optimal bridge RC values may be varied in terms of the impedance characteristics of the PCB layout. Some CH7036 register setting changes may be required in terms of the bridge construction, refer to **Table 3**.



(a) Typical RC bridge for each differential pair **(b) Recommended bridge for each differential pair**

Figure 12: The connection of the HDMI outputs

Table 3: Register change list when using 240 Ω terminal resistors

Address	Value
R2_0Ah	0x03

R2_0Bh	0xED
R2_0Ch	0x74
R2_0Dh	0x51

• HDMI Link Clock Outputs (TLC and TLCB)

These pins provide the HDMI differential clock outputs for HDMI corresponding to data on the TDC [2:0] and TDCB[2:0] outputs (Refer to **Figure 12**).

• HPD (HDMI Hot Plug Detect)

This input pin determines whether the HDMI link is connected to a HDMI panel, it should be pulled low with a 47 k Ω resistor. When the panel is connected, the HPD will be given a voltage greater than 2.4 volts.

• SCL and SDA (DDC bus)

The Display Data Channel is used by CH7036 to determine the capabilities and characteristics of the Panel by reading the E-EDID data structure. These two pins should be connected to DDC_SD and DDC_SC of CH7036, and pull up to 5V with 1.8 KΩ resistors.

2.9 LVDS Output Pins

• LVDS output Pins

CH7036 can Output 18bit or 24bit SPWG format data for LVDS Panel, as shown in **Figure 13**. Since those signals are differential, they must be routed in pairs. The Differential impedance of differential lines should be the same with the Panel termination resistor.

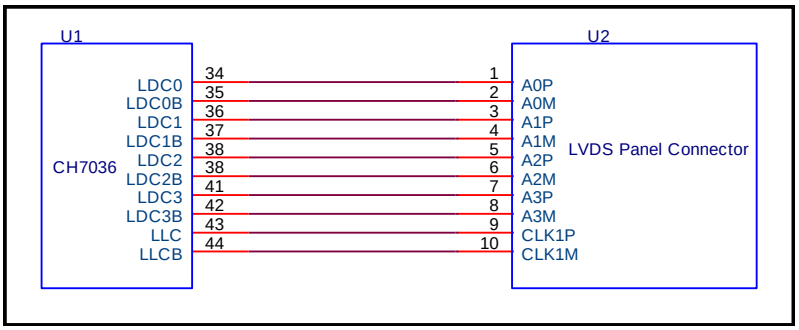


Figure 13: The connection of the HDMI outputs－CH7036 HDMI connectors

• PWM

This pin is for Backlight brightness adjustment. It has a default output 3.3V CMOS level. It output a square waveform, and its duty-cycle as well as frequency can be adjusted through the Register.

2.10 RGB Output Pins

• DAC0~2

Three on-chip 10-bit high speed DACs provide RGB output. If the DACs require a double termination, a 75 Ω resistor should be placed between each DAC pin and the ground as shown in **Figure 14**.

• HSO and VSO

The HSO and VSO are COMS output Pins, the voltage level is the same with AVDD. The buffer, 74ACT08, have level shift function. It should be used to make sure CH7036 can drive monitor properly.

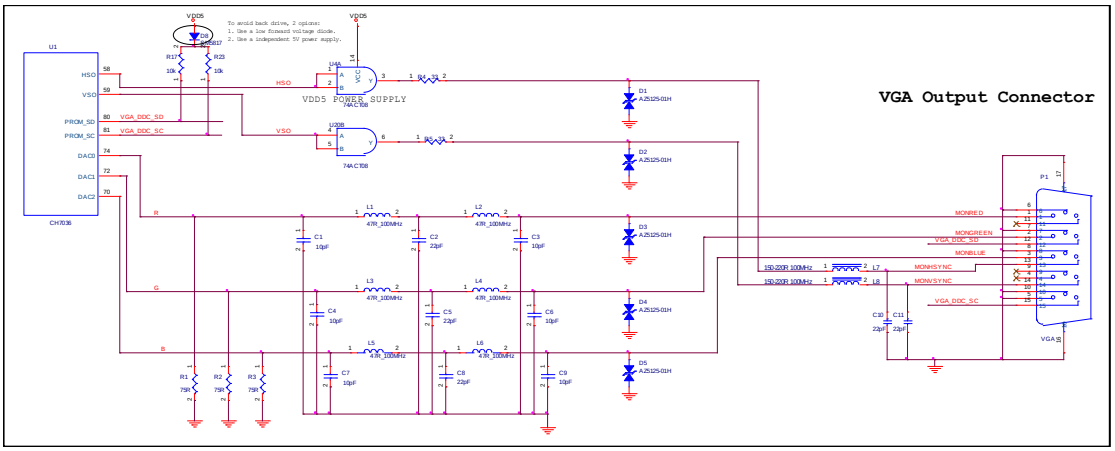


Figure 14: The CH7036 RGB outputs

2.11 Thermal Exposed Pad Package

The CH7036 is available in 88-pin QFN package with thermal exposed pad package. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7036.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 15**.

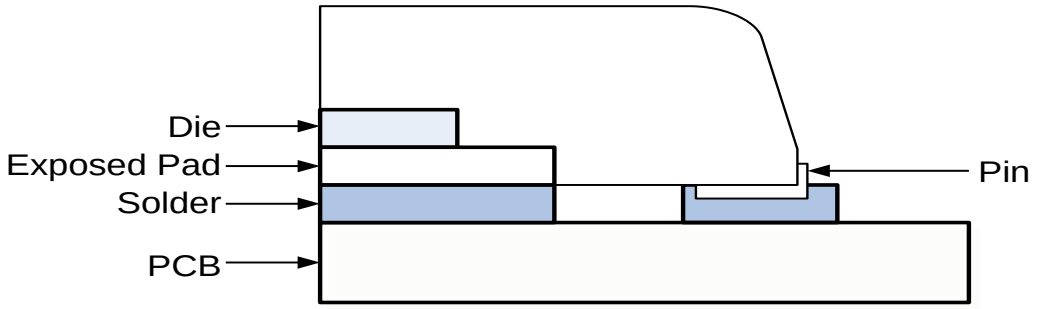


Figure 15: Cross-section of exposed pad package

Thermal pad dimension is from 6.6mm to 6.9mm (min to max), 6.6mm x 6.6mm is the minimum size recommended for the thermal pad, and 6.9mm x 6.9mm is the maximum size. As shown in **Figure 16**, the thermal land pattern should have a 5x5 grid array of 1.0 mm pitch thermal vias connected to the ground layer of the PCB. These vias should be 0.3mm in diameter with 1 oz copper via barrel plating.

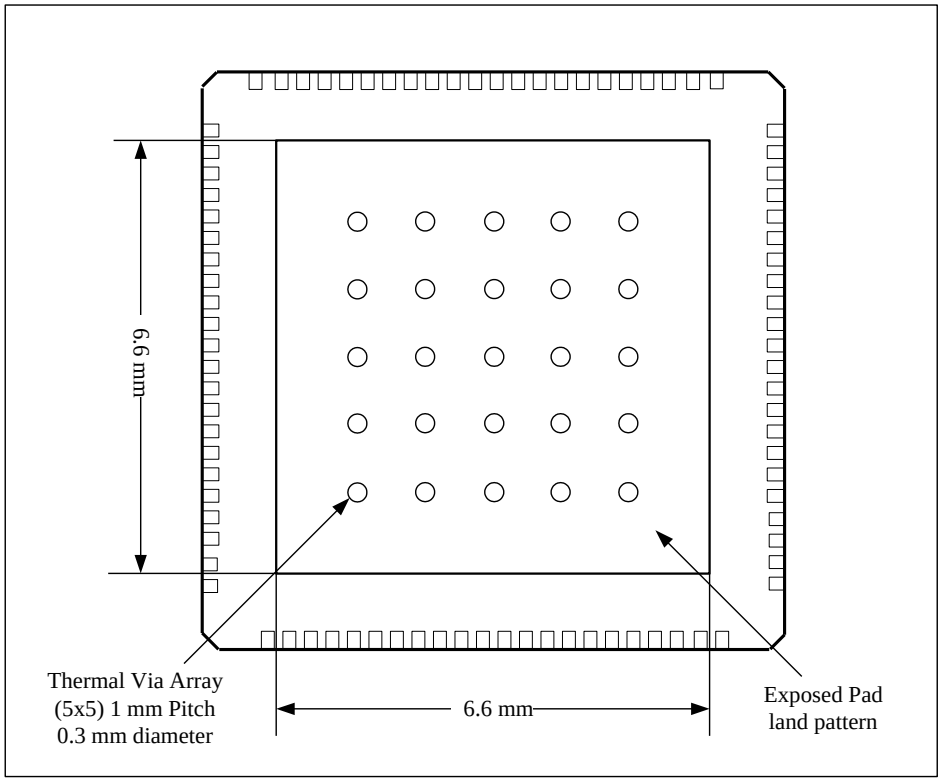


Figure 16: Thermal Land Pattern

When applying solder paste to the thermal land pattern, the recommended stencil thickness is from 5 to 8 mils. Thermal resistance was calculated using the thermal simulation program called ANSYS.

2.12 QFN Package Assembly

For the assembly process, it is important to limit the amount of solder paste that is put under the thermal pad. If too much paste is put on the PCB, the package may float during assembly. Compared with the solder mask of thermal pad, the paste mask should be shrank to70%~80%. **Figure 17** shows a paste mask pattern in gray for the thermal pad.

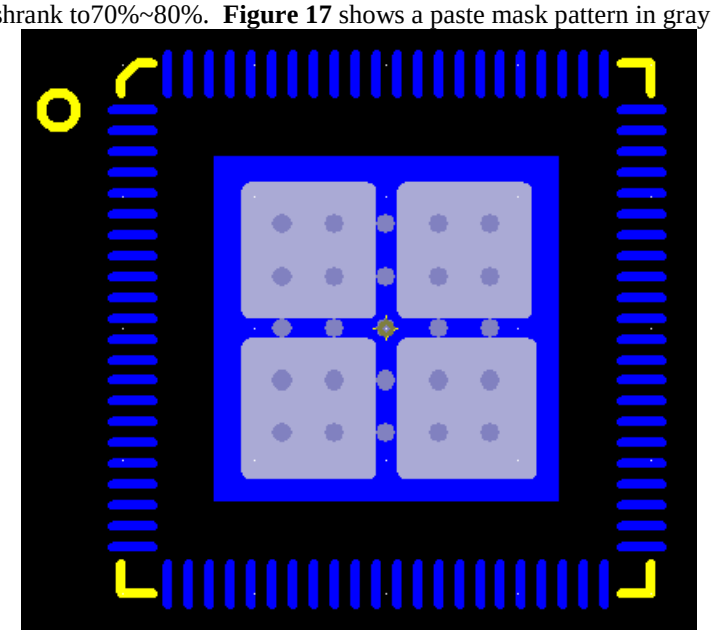
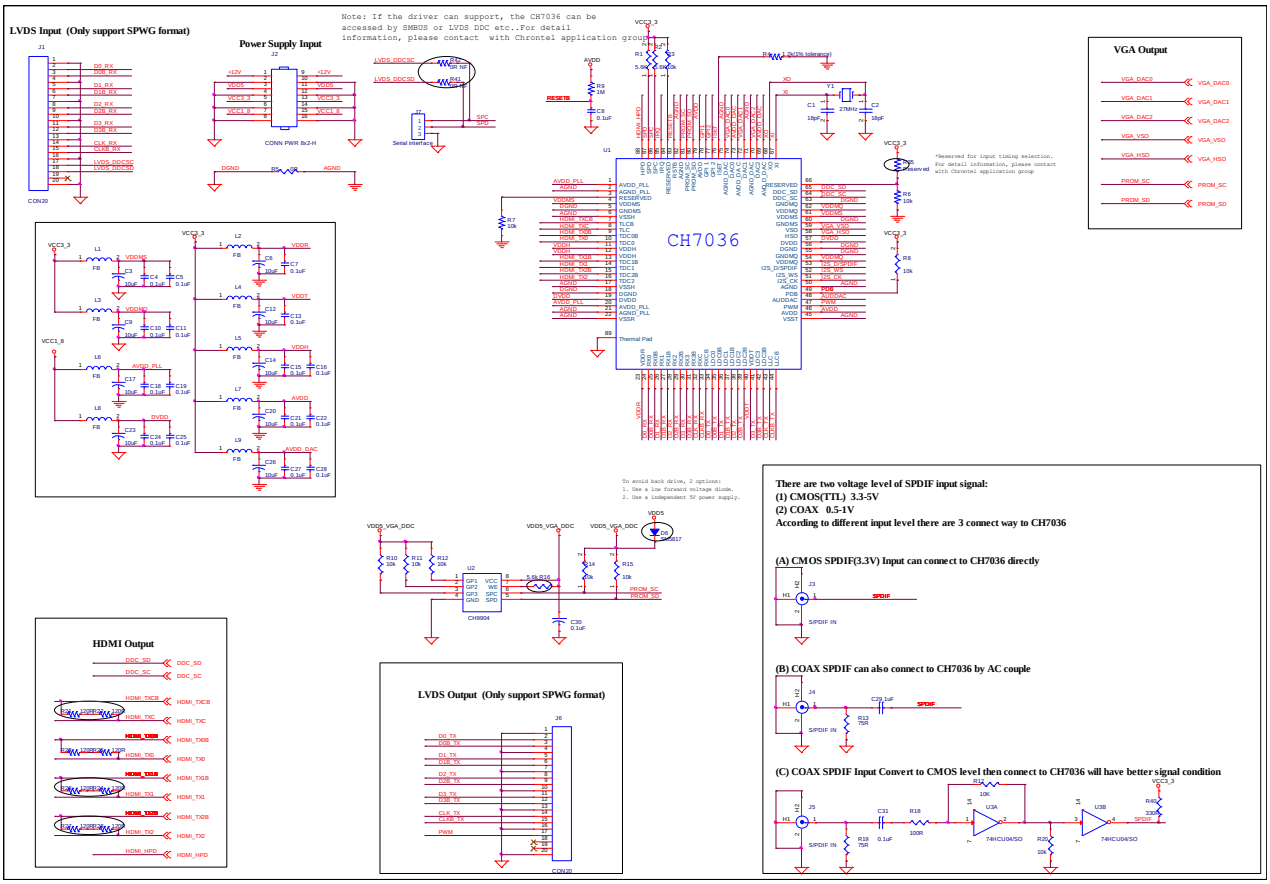


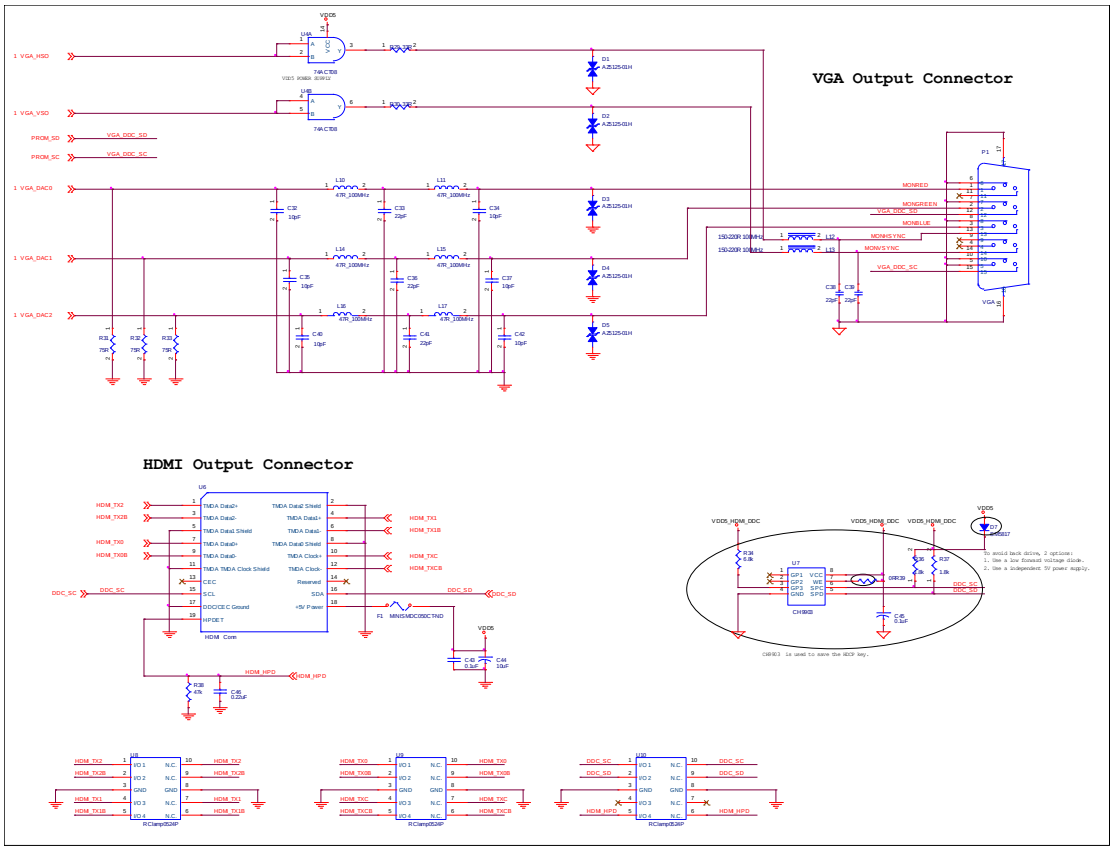
Figure 17: Thermal Pad Paste Mask Pattern

3.0 Reference Design Example

The figures below are the reference schematic of CH7036, which is provided here for design reference only. **Table 4** provides the BOM list for the reference schematic.

3.1 Reference Schematic





3.2 Reference Board Preliminary BOM

Table 4: CH7036 Reference Design BOM List

Item	Quantity	Reference	Part
1	5	D1, D2, D3, D4, D5	AZ5125-01H
2	2	C1, C2	18 pF
3	10	C3, C6, C9, C12, C14, C17, C20,	10 µF
		C23, C26, C44	
4	21	C4, C5, C7, C8, C10, C11, C13, C15	0.1 µF
		C16, C18, C19, C21, C22, C24, C25	
		C27, C28, C30, C31, C43, C45	
5	1	C29	1 µF
6	6	C32, C34, C35, C37, C40, C42	10 pF
7	5	C33, C36, C38, C39, C41	22 pF
8	1	C46	0.22 µF
9	2	D6, D7	SM5817
10	1	F1	MINISMDC050CT-ND
11	2	J1, J6	CON20
12	1	J2	CONN PWR 8x2-H
13	3	J3, J4, J5	S/PDIF IN
14	9	L1, L2, L3, L4, L5, L6, L7, L8, L9	FB
15	6	L10, L11, L14, L15, L16, L17	47R_100MHz
16	2	L12, L13	150-220R 100MHz

17	1	P1	VGA
18	3	R1, R2, R16	5.6 kΩ
19	11	R3, R6, R7, R8, R10, R11,	10 kΩ
		R12, R14, R15, R17, R20,	
20	1	R4	1.2 kΩ (1% tolerance)
21	2	R5, R39	0 Ω
22	5	R13, R19, R31, R32, R33	75 Ω
23	1	R9	1 MΩ
24	1	R18	100 Ω
25	8	R21, R22, R23, R24, R25, R26, R27, R28	120 Ω
26	2	R29, R30	33 Ω
27	1	R34	6.8 kΩ
28	2	R36, R37	1.8 kΩ
29	1	R38	47 kΩ
30	1	R40	330 Ω
31	1	R35	reserved
32	1	U1	CH7036A
33	1	U2	CH9904
34	1	U3	74HCU04/SO
35	1	U4	74ACT08
36	1	U6	HDMI Connector
37	1	U7	CH9903
38	2	U8, U9, U10	RClamp0524P
39	1	Y1	27MHz

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